

**SWITCHING  
N-CHANNEL POWER MOS FET  
INDUSTRIAL USE**

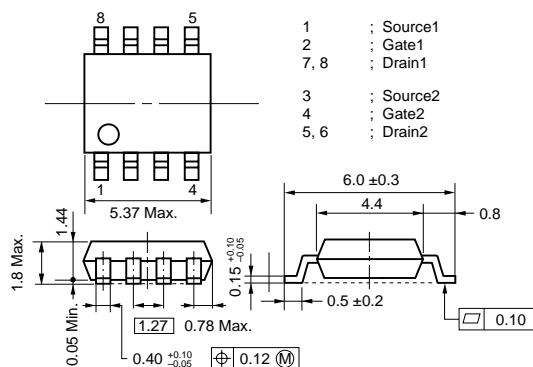
**DESCRIPTION**

The μPA1760 is N-Channel MOS Field Effect Transistor designed for DC/DC Converters and power management application of notebook computers.

**FEATURES**

- Dual Chip Type
- Low On-Resistance
- ★  $R_{DS(on)1} = 26.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 4.0 \text{ A)}$
- ★  $R_{DS(on)2} = 36.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 4.0 \text{ A)}$
- ★  $R_{DS(on)3} = 42.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.0 \text{ V, } I_D = 4.0 \text{ A)}$
- Low  $C_{iss}$  :  $C_{iss} = 760 \text{ pF TYP.}$
- Built-in G-S Protection Diode
- Small and Surface Mount Package (Power SOP8)

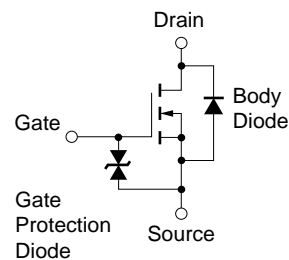
**PACKAGE DRAWING (Unit : mm)**



**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C, All terminals are connected.)**

Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	30	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	±20	V
Drain Current (DC)	I <sub>D(DC)</sub>	±8.0	A
Drain Current (Pulse) <sup>Note1</sup>	I <sub>D(pulse)</sub>	±32	A
Total Power Dissipation (1 unit) <sup>Note2</sup>	P <sub>T</sub>	1.7	W
Total Power Dissipation (2 unit) <sup>Note2</sup>	P <sub>T</sub>	2.0	W
Channel Temperature	T <sub>ch</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	-55 to + 150	°C
★ Single Avalanche Current <sup>Note3</sup>	I <sub>AS</sub>	8	A
★ Single Avalanche Energy <sup>Note3</sup>	E <sub>AS</sub>	6.4	mJ

**EQUIVALENT CIRCUIT  
(1/2 Circuit)**



**Notes 1.**  $PW \leq 10 \mu s$ , Duty cycle  $\leq 1 \%$

- ★ **2.** T<sub>A</sub> = 25 °C, Mounted on ceramic substrate of 2000 mm<sup>2</sup> x 1.6 mm
- ★ **3.** Starting T<sub>ch</sub> = 25 °C, R<sub>G</sub> = 25 Ω, V<sub>GS</sub> = 20 V → 0 V

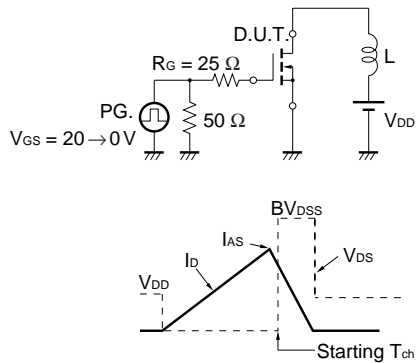
**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage Exceeding the rated voltage may be applied to this device.

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

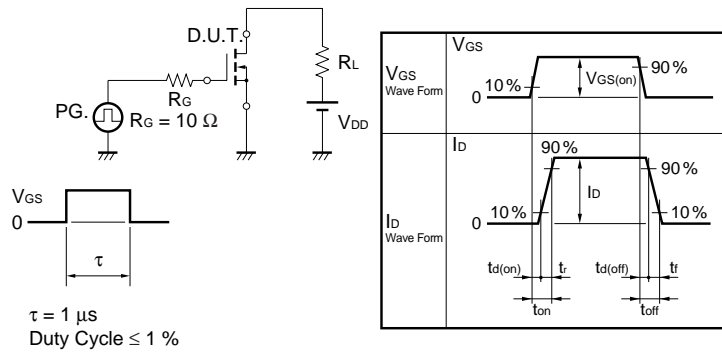
★ ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4.0 A		20.5	26.0	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 4.0 A		27.0	36.0	mΩ
	R <sub>DS(on)3</sub>	V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 4.0 A		31.0	42.0	mΩ
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.5	2.1	2.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 4.0 A	3.0	7.5		S
Drain Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			10	μA
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±16 V, V <sub>DS</sub> = 0 V			±10	μA
Input Capacitance	C <sub>iSS</sub>	V <sub>DS</sub> = 10 V		760		pF
Output Capacitance	C <sub>oSS</sub>	V <sub>GS</sub> = 0 V		250		pF
Reverse Transfer Capacitance	C <sub>rSS</sub>	f = 1 MHz		95		pF
Turn-on Delay Time	t <sub>d(on)</sub>	I <sub>D</sub> = 4.0 A		20		ns
Rise Time	t <sub>r</sub>	V <sub>GS(on)</sub> = 10 V		140		ns
Turn-off Delay Time	t <sub>d(off)</sub>	V <sub>DD</sub> = 15 V		50		ns
Fall Time	t <sub>f</sub>	R <sub>G</sub> = 10 Ω		30		ns
Total Gate Charge	Q <sub>G</sub>	I <sub>D</sub> = 8.0 A		14		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>DD</sub> = 24 V		2.0		nC
Gate to Drain Charge	Q <sub>GD</sub>	V <sub>GS</sub> = 10 V		5.0		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 8.0 A, V <sub>GS</sub> = 0 V		0.86		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 8.0 A, V <sub>GS</sub> = 0 V		30		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100A/μs		20		nC

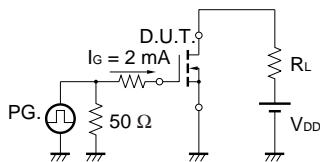
TEST CIRCUIT 1 AVALANCHE CAPABILITY



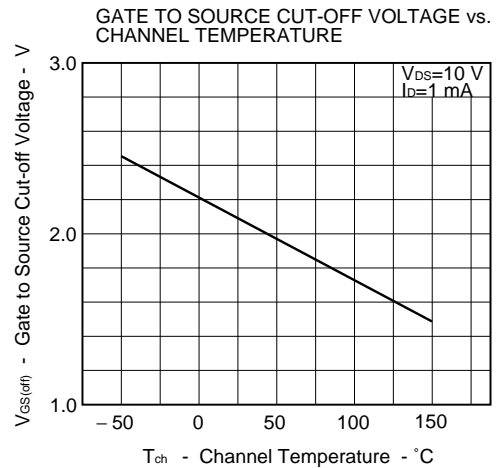
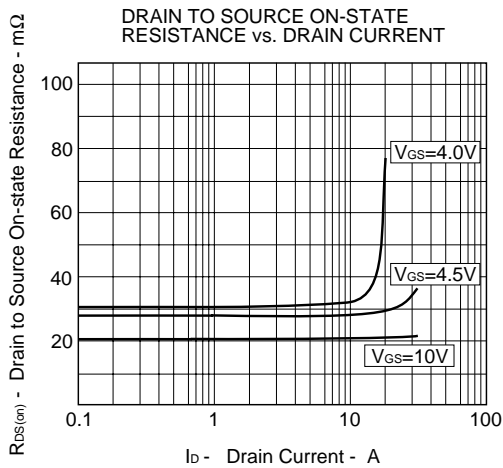
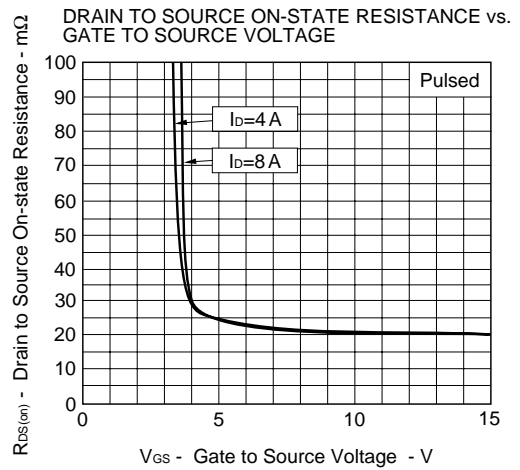
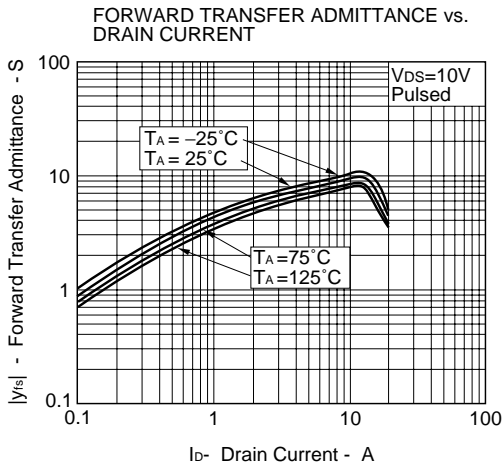
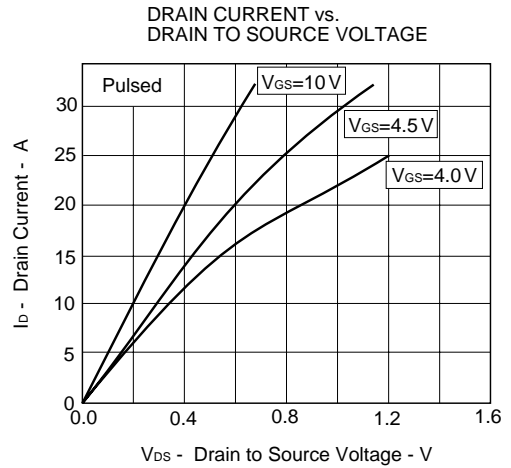
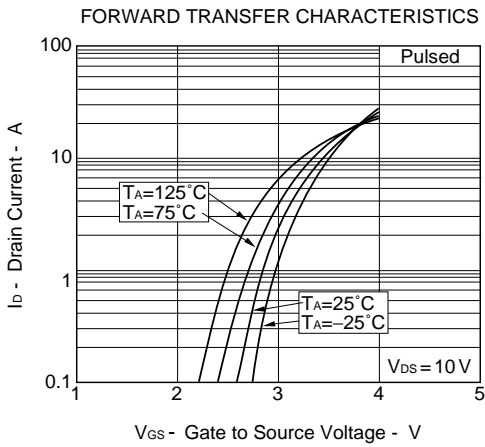
TEST CIRCUIT 2 SWITCHING TIME

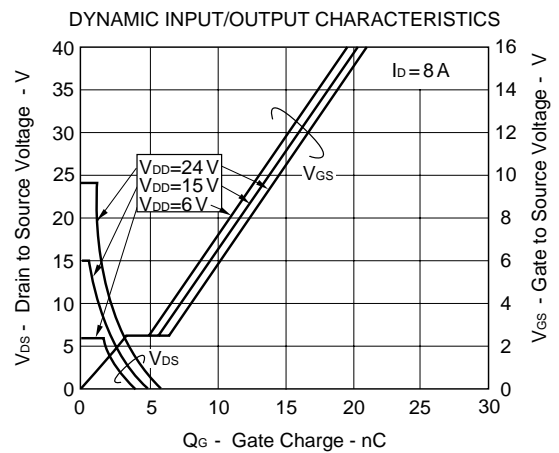
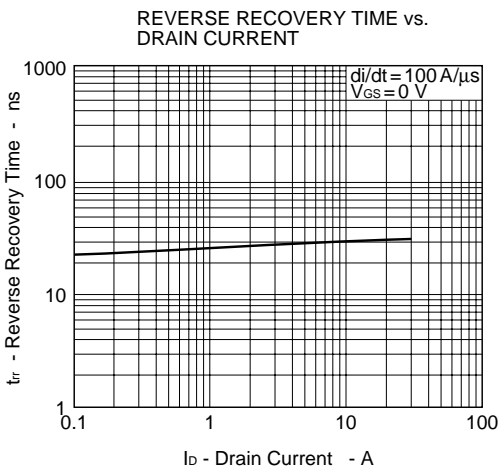
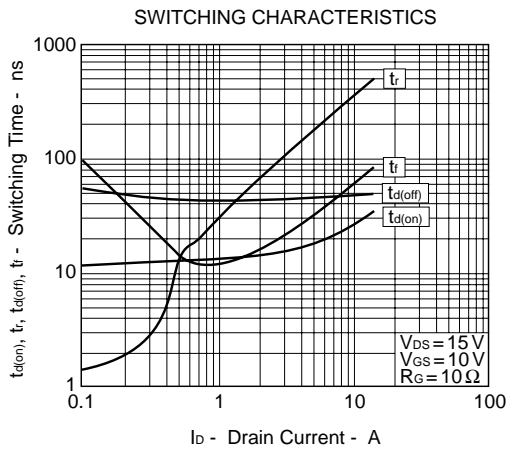
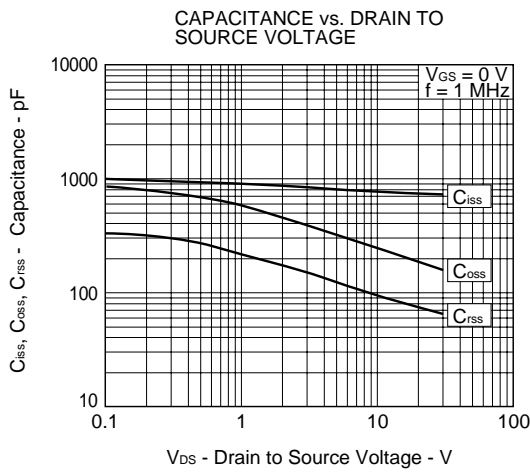
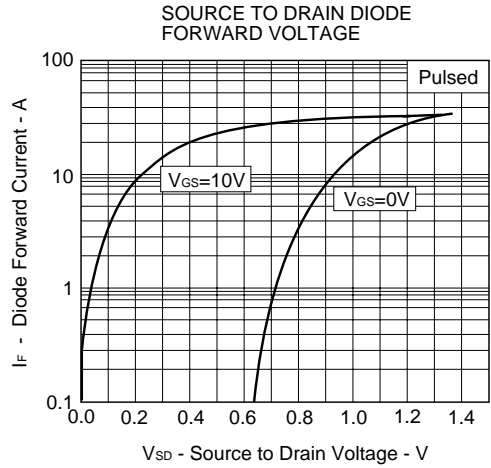
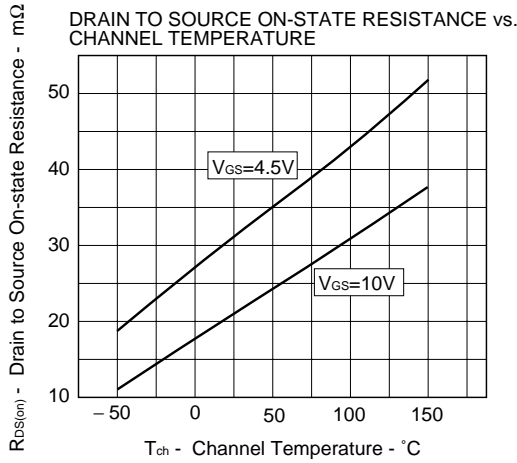


TEST CIRCUIT 3 GATE CHARGE

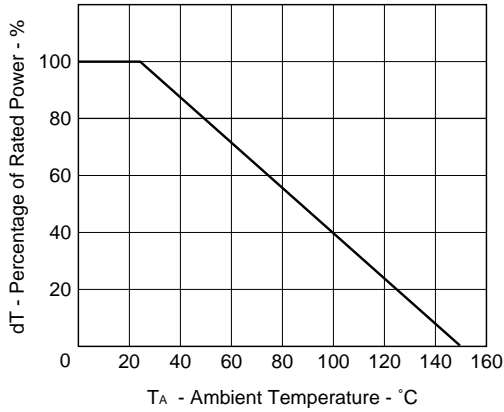


★ TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

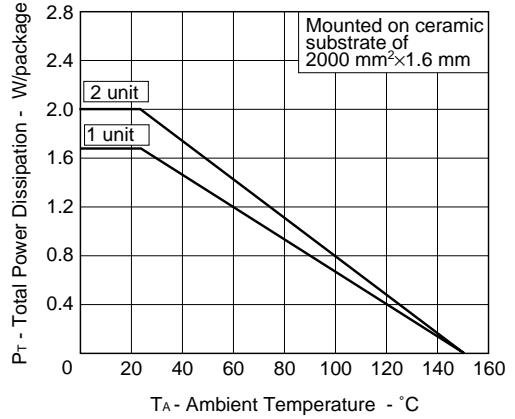




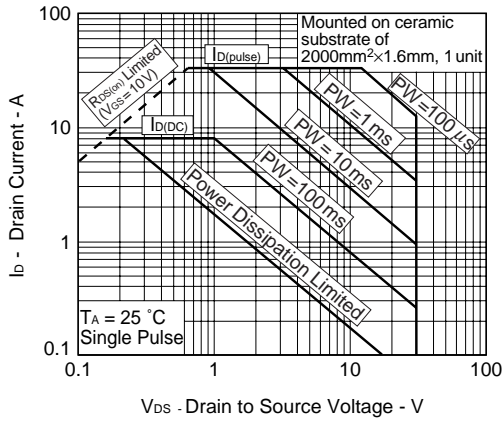
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



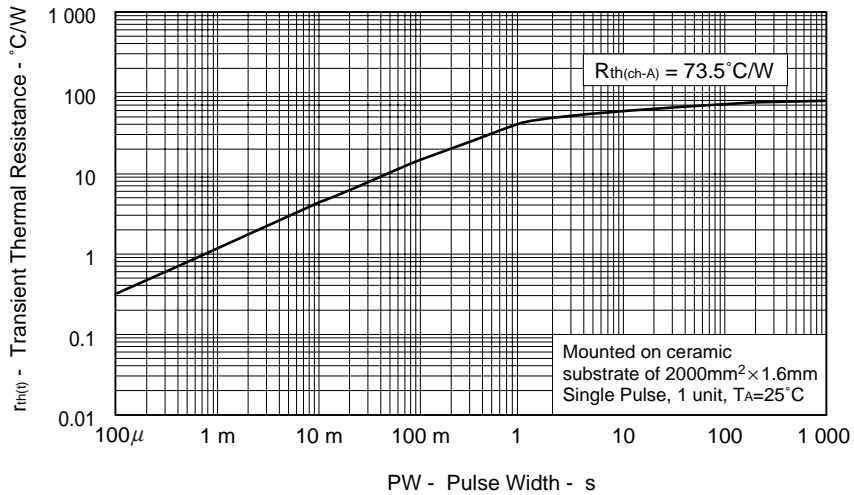
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE

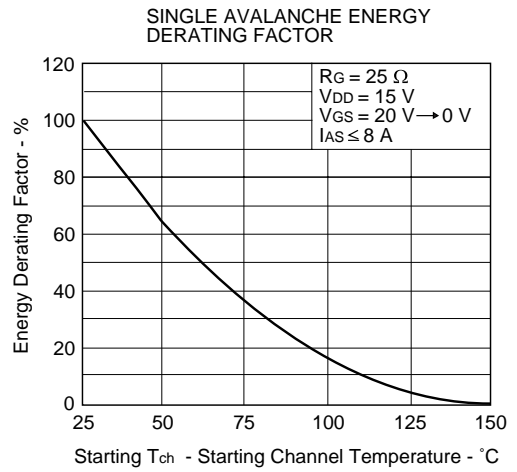
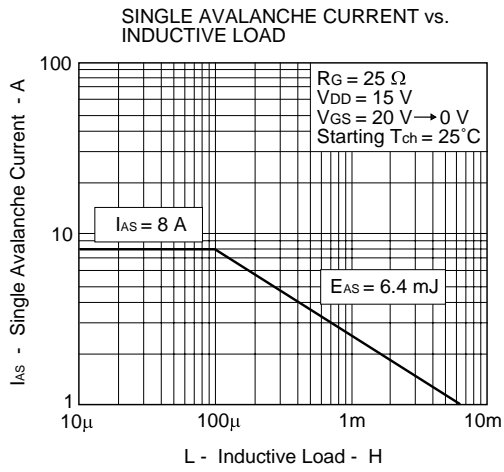


FORWARD BIAS SAFE OPERATING AREA



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH





[MEMO]

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